31st January 2025

Session 3 meeting minutes

# Introduction

Began with doubts in previous discussion and assignments progress update.

1)Introduction to AMS verification.

- Why there is a need of AMS verification?

Complexity of chip is increasing due to evolving technology. Demand of AMS chips in market is increasing. Hence the AMS verification is popularizing in market in recent years.

# Assignment

1. Continuation of digital clock assignment.

# Discussion

1. Began with types of verification.

1) Analog verification – Chip containing Analog blocks are verified in this process.

2) Digital verification – digital blocks on chip are verified in this process

3) Analog mixed signal verification.

1. Started with ‘Why AMS verification in necessary?’
2. Analog signal – Continuous time signal (Electrical signal). It is slow, steady and detailed.
3. Digital signal – Discrete time signal. (Logic). It is faster compared to analog signal and does not have continuous value.
4. As analog block is slower than digital, when we use digital block to trigger analog block, it will disturb the function of analog block and vice versa. So, there is a need of an AMS verification to analyse and resolve this behaviour.
5. Question- How do we resolve it.

Using Deglitchers. Deglitcher block will remove both positive and negative glitches from the circuit.

We need to think whether we the glitch is affecting our design and if it is then we need to remove it.

1. Clock domain crossing

If different clock signals need to interact then we have to use synchronizers to synchronize them. For that we can use FIFO or handshake mechanism.

1. Connect modules – Used to connect analog blocks to digital and vice versa.

(It is automatically inserted by tool or we can design it for specific requirement).

1. Verification environment-In this we mimic the real environment where chip is going to work.

We use system Verilog or UVM to create verification environment.

\*Understand the product.

1. Effort Estimation- Estimating duration, people and tools required for the project.
2. Verification plan / Test plan-

SRAM



en

clk data\_in

rst

wr data\_out

addr

1. Test name-

E.g. 1) enable- disable 2) reset

1. Test Intentions- Single line information about Test name.
2. Test description -To fulfil Test Intensions, how are you going to process further (It can be larger).

E. g. 1) provide VDD=5v 2) provide en=0

1. Result – Pass/Fail.

3) Modelling-

Tools are conceptual. They are based on approximation methods like Newton- Raphson methos, Euler’s methos, KCL, KVL and Ohm’s law etc.

Simulators – 1) Analog – spectre

2) Digital – xrun, irun

Major concern in AMS is simulation time as analog signal is continuous.

\*To reduce simulation time-

1. settings

1. Conservative - apply calculations to all the points.
2. Liberal - apply calculations to very few points.
3. Moderate- apply calculations to moderate no. of points.
4. Use of digital clock.
5. Modelling- Explained modelling with below example

A1

A0

---------------------------------------------------

A99

Above fig. shows chip containing multiple analog blocks. It will require larger simulation time.

Here, It we have to apply test cases to A1 block only, then running simulation for all blocks will increase simulation time. Hence we remove others blocks from schematics and write Verilog code for them (Behavioural modelling) .

4) EDA tool information- Electronic Design Automation.

Mainly consist three software.

1)cadence

2)synopsys – mainly used for physical design. (VCS)

3)mentor- calibre, Questa-sim.

# Conclusion

1. Discussed verification types and need of AMS verification.
2. Verification plan / Test plan.
3. Introduction to the concept of Modelling.